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Date December 20, 2005

To Examiner Vineeta S. Panwalker

Of USPTO Group Art Unit 2631

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From Ronald Kimble

Subject Comments on Examiner's Amendment in Notice of Allowance

Our Ref Q68642

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(including cover sheet)

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Re: U.S. Application No. 10/090,749 Atty. Docket Q68642

Dear Examiner Panwalker:

Thank you for agreeing to review Applicants' comments on why Figure 3 of the subject application does not require amendment. I hope that after you consider Applicants' comments, that a supplemental Notice of Allowability could be issued removing the Examiner's Amendment.

Applicants understand that the Examiner's proposed amendment of Figure 3 requires that at all times $PM \cdot KM$ and PD are input into one comparator COMP1 (the one shown on the top part of Figure 3) and also at all times $PD \cdot KD$ and PM are input into the other comparator COMP1 (the one on the lower part of Figure 3).

The first comparison is represented at the right hand side of the flow chart of Figure 4 and the second comparison is represented at the left hand side of the flow chart of Figure 4. It is noted that KD and KM may each assume any "constant positive" value.

Figure 3 as originally filed requires that at all times $PM \cdot KM$ and $PD \cdot KD$ are input into both comparators COMP1 (upper and lower). Here again KM and KD may assume any "constant positive" value. Thus if KD is set to one and KM is set to a different value the input at the upper comparator would be $PM \cdot KM$ and PD . The same input would be present at the lower comparator. This is in accordance with the invention because in this case (comparing PD with $PM \cdot KM$) the comparison is done assuming that "at the preceding time of processing, the signal that was driving the clock circuit was the Main one" (pg. 8, lines 13-14). Thus, if the Main signal was driving the clock circuit, there is no need to compare PM with $PD \cdot KD$ (which would be required for the case where the Diversity signal was driving the clock circuit).

Furthermore, the flow chart of Figure 4 shows a first (top) block in which the condition of "at the preceding time of processing, the signal that was driving the clock circuit was the Main one or not" is being checked. If the answer is yes, then the steps of the right hand side of the flow chart are followed. Otherwise, the left hand side procedure is followed in which case KM is set to one and KD is set to a different value (and the comparison would be analogous to that of the previous case). The flow chart of Figure 4 only allows for one option of comparison, i.e. either the right hand side or the left hand side. This is in accordance with the configuration shown in the original Figure 3. The proposed amended version of Figure 3 may allow for both options of comparison and thus, an additional control action may be required to activate only one of the comparison options or disable the other.

It is in fact noteworthy that in the original Figure 3, the same reference numeral is assigned to both, the upper and the lower comparators, i.e. COMP1; which may be interpreted as meaning that only one comparator may suffice to perform the comparison (as stated above, Figure 4 only allows for one option of comparison). This is in line with

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the above interpretation of the original Figure 3 because the same inputs (PM*KM and PD*KD) are present at all times in both, the upper and the lower comparators, COMP1.

Therefore, Applicants respectfully submit that the original Figure 3 is in accordance with the teaching of the invention in view of the description and Figures (in particular Figure 4, noting that the specification describes these Figures together).

Thank you for your consideration.

Best regards,
Ron Kimble

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